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Comparative Study of Proposed 4T SRAM With convention 4T and 6T SRAM Using 45nm Technology

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Abstract: *Static random access memory (SRAM) is an important component of embedded cache memory of handheld digital devices. SRAM has become a major data storage device due to its large storage density and less time to access. Exponential growth of low power digital devices has raised the demand of low power SRAM. This paper compares the performance of proposed 4-Transistor(4T) SRAM design with the conventional 4-Transistor (4T) and 6-Transistor (6T) SRAM in 45nm standard CMOS process technologies. These SRAM cells are designed with a width of 45nm and length of 120nm in 45nm technology . The simulation has been done in the Cadence Virtuoso environment. In accordance with the results obtained, the proposed 4T SRAM cell in 45nm CMOS technology has low power dissipation value and lower static noise margin (SNM) compared to the conventional 4T SRAM and 6T SRAM*

Keywords: Static Random Access Memory (SRAM), 4-transistor (4T) SRAM, 6--Transistor (6T) SRAM, CMOS process technologies, SNM

I. INTRODUCTION

Semiconductor memory arrays can store a lot of data in a variety of digital systems. Number of transistors are used more for storage than for logic operations and other uses. Compact size and fabrication technology have been driven by the growing need for large storage capacity. Every two years, the semiconductor memory array's data storage capacity roughly doubles. An important factor to consider for design that affects the memory array's overall storage capacity is its area efficiency, or the number of storage bits per unit area.

The time needed to store and retrieve data in a memory array is a crucial consideration. SRAM (Static Random Access Memory)is utilized in the CPU register, router buffer, hard drive buffer, and certain printers.

II. 6T SRAM CELL

The 6T SRAM cell utilizes six transistors to store a single bit of information. It comprises two cross-coupled CMOS inverters, implemented using four transistors, which form a bistable latch for data retention. The remaining two transistors function as access transistors, enabling controlled read and write operations by connecting the storage nodes to the bit lines during word line activation.

The word line (WL) governs access to the SRAM cell by enabling or disabling the access transistors, while the bit lines (BL and BLb) facilitate data transfer during read and write operations. At the core of the 6T SRAM cell are two cross-coupled CMOS inverters that form a bistable latch. This bistable configuration allows the cell to stably maintain one of two logic states, representing binary '0' or '1'.

The two access transistors (M1 and M2) are used to connect the internal storage nodes (A and B) to the bit lines (BL and BLb) when the word line (WL) is active.

Hold State:When the word line is low (WL = 0), the access transistors are off, isolating the cell and preserving its stored data.

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Write Operation: To write a new value, the bit lines (BL and BLb) are set to the desired values (e.g., BL = 0, BLb = 1), and the word line is raised to high (WL = 1). This connects the bit lines to the inverters, overwriting the existing data with the new values.

Read Operation: To read the stored data, the word line is raised (WL = 1), and the access transistors are turned on. The bit lines reflect the stored data, with BL being the value of node A and BLb being the value of node B

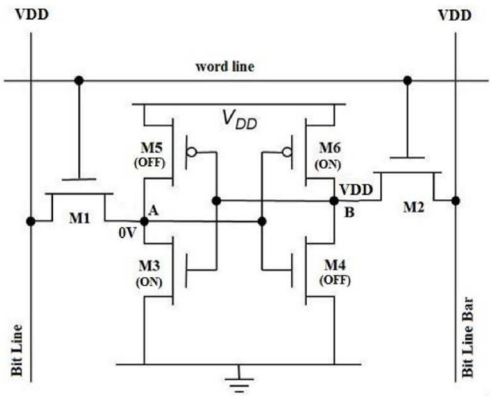

Figure 2.1 – 6T SRAM cell

4T SRAM CELL

A 4T SRAM (Static Random Access Memory) cell utilizes four transistors to store one bit of data. It functions by employing two cross-coupled inverters to maintain the data state (either a '1' or a '0') as long as power is supplied. Read and write operations are performed by selectively activating access transistors connected to bit lines, allowing data to be accessed or modified.

Hold Operation: The cross-coupled inverters ensure that once a state (either high or low voltage) is established at the output node of one inverter, it is maintained, thereby storing the data bit.

Read Operation: The word line is activated, turning on the access transistors. This connection allows the bit lines (BL and BLb) to sense the voltage at the internal nodes of the inverter, indicating the stored data. A sense amplifier detects the voltage difference on the bit lines and amplifies it to produce a readable output.

Write Operation: The word line is activated, and the desired data (and its complement) is driven onto the bit lines. This action forces the internal nodes of the inverters to the desired voltage levels, effectively overwriting the previous data.

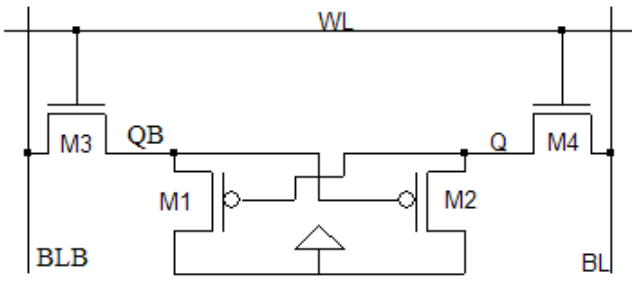

Figure 2.2 – 4T SRAM cell

Proposed 4T SRAM Cell

The proposed 4T SRAM cell[1] which integrates an inverter as illustrated in figure , is designed without a direct connection to the supply voltage (Vdd) [3]. While a considerable portion of on-chip memory is utilized for transient or short-lived data storage, the majority of on-chip array architectures continue to adopt 4T SRAM cells due to their ability to retain data indefinitely. This architectural choice reflects a tradeoff between power efficiency and data retention requirements, even in applications where long-term data storage is not always necessary.

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This makes 4T cells uniquely well-suited for predictive structures like branch predictors and BTb where data integrity is not essential.

The proposed 4T SRAM cell model [1] has been implemented, and its write functionality has been evaluated under differential input conditions facilitated by an inverter-based input scheme. A single data input source is employed to simultaneously drive both the bit line (BL) and its complement (BLb), ensuring differential signaling. For successful data write, the word line (WL) must undergo a logic transition—either a rising edge (0 → 1) or a falling edge (1 → 0)—during the application of the input, enabling the access transistors to latch the intended data state into the cell.

III. MODELING AND RESULTS

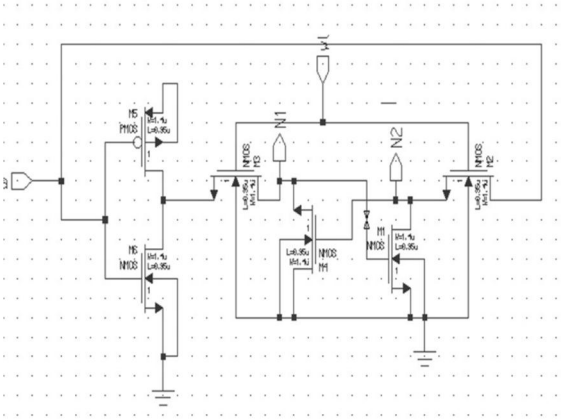

Figure 3.1 – Proposed 4T SRAM cell

IV. MODELING RESULTS

The new 4T SRAM cell has more power efficiency so it is useful for the design of memories in power efficient applications. Without affecting the stored bit the maximum DC voltage can be condoned by the proposed SRAM cell. These SRAM cells are designed with 45nm technology, width of 45nm and length of 120nm.

The SNM can be achieved by DC analysis. Calculating the delay for each SRAM cell in 180nm, 90nm, 45nm technology. Delay time depends on the critical voltage and W/L ratio of the transistors. In this work, the supply voltage considered is 0.5 V.

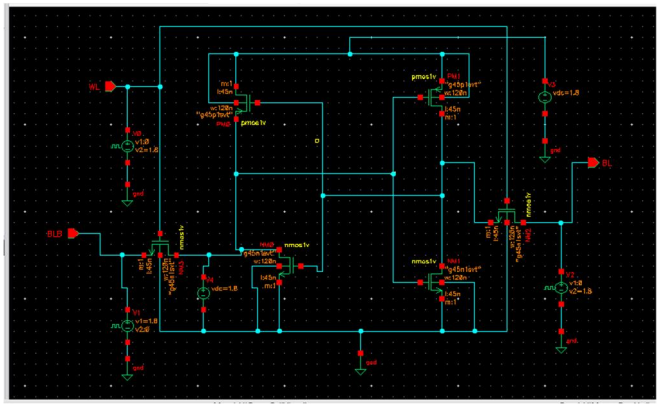

Figure 4.1 – 6T SRAM cell

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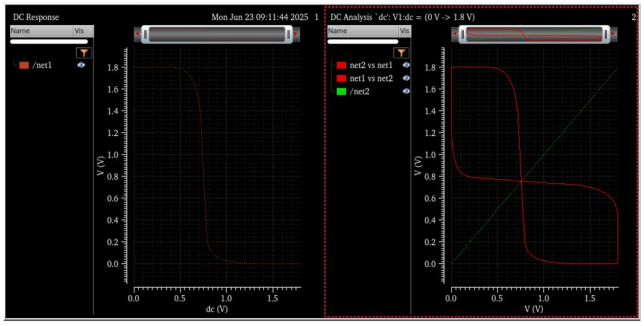

Figure 4.2 – 6T SRAM cell dc analysis 45nm process technology

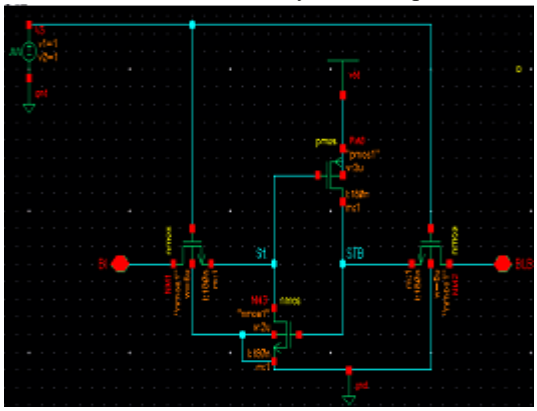

Figure 4.3 – 4T SRAM cell

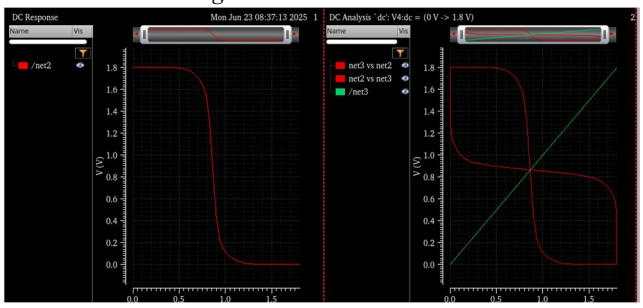

Figure 4.2 – 4T SRAM cell dc analysis 45nm process technology

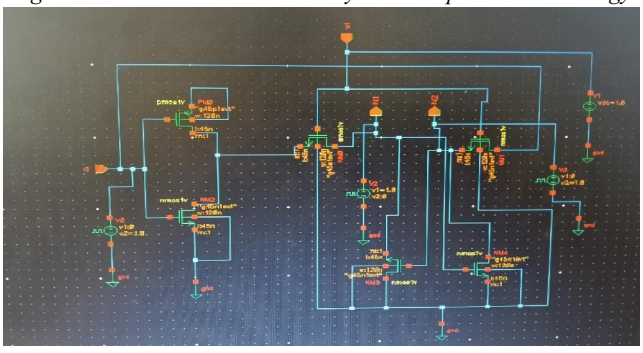

Figure 4.4 – Proposed 4T SRAM cell

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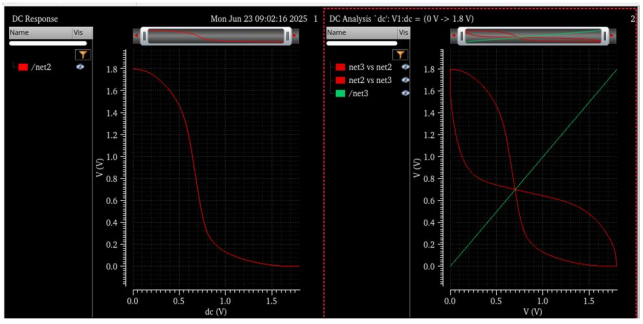

Figure 4.2 – Proposed 4T SRAM cell dc analysis 45nm process technology

PARAMETER	4T	Proposed 4T	6T
Area	18.89	24.03	80.24
SNM for read operation	0.23V	0.21V	0.31V
SNM for write operation	0.29V	0.25V	0.35V
Power dissipation	478.24nW	658.33nW	519.7 nW

Table 4.1 – Performance Comparison of 4T, proposed 4T, 6T SRAM cell 45nm technology

V. CONCLUSION

In this paper the simulation is done by using Cadence Virtuoso tool. The simulation is done for 4T, proposed 4T and 6T SRAM cells in 45nm process technology. The proposed 4T SRAM Cell is designed using conventional and an inverter to achieve high reliability and high density SRAM. The proposed SRAM cell power dissipation, and occupies less area when compared to the 6T SRAM cell. As the Proposed Model dissipates higher power compared to the other SRAM cell while the SNM for read and write operation for the proposed model is less compared to the other SRAM cell.

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